



## **Hot Carrier Injection:**

### ***Introduction:***

In high current device, when the average carrier high enough ( $> 1.1\text{eV}$ ), the carriers in channel will has possibility to inject to the oxide where they can be trapped at the interface (normally electrons). At same time, high energy carriers will create n-p pairs through impact ionization. In nMOS, the generated electrons will be collected by drain and holes will drift to substrate contact occurring a substrate current. This current is an indicator of the energy of the carriers and sensitivity of the device to hot carriers degradation.

### ***The effect of HCI***

Hot-Carrier Injection (HCI) degradation slows down circuit speeds that can potentially cause circuit operating failures. HCI arises as a result of the aggressive scaling of device geometries, most notably device channel lengths. Shorter channel lengths mean higher circuit speeds, but they also increase electric fields in the channel. These fields can damage the gate oxide interface, resulting in degradation in device performance. The injection of carriers into the oxide results in a change of I-V characteristic. Under AC condition, the stress effects are similar to the DC condition. AC stress degradation normally is larger than the DC.

### ***Test description:***

This stress test measures the resistance of the oxide on the devices to trapping charge (electron). A measure of 10% change in transconductance ( $g_m$ ) is generally used as failure point in this stress. This stress is typically done on single transistors with a DC voltage. It can be used as a relative measure of how easily the devices transistors are affected by hot electrons. The degradation of transistors typically manifests itself as a shift in the characteristic  $I_d$ - $V_g$  performance. During operation at high current/voltage, measurements of several transistor characteristics are performed in both the linear and saturation modes:

-Transconductance; drain current; threshold voltage; substrate current; subthreshold swing are measured.

*Test requirements:* the equipment should be able to measure current for 1nA with resolution of at least 10pA.

### ***Input parameters:***

Defined- Drain current limit, Gate current limit, Device type (N, P-channel),

Stress- temperature,  $V_d$ ,  $V_g$ ,

Stress timing-Set up the duration of thee stress.

Stress store- Control the data storing during stress.

EOT (End of test),



**Test Output:**

$I_d$  Vs  $V_{gs}$ ,  $V_{ds}$ ,  $I_g$  Vs.  $V_{gs}$ ,  $I_{sub}$  Vs.  $V_{gs}$ ,  $g_m$  Vs  $V_{gs}$ ,  $I_d$  Vs T

\* Transconductance ( $g_m$ ) is the change in drain current verse the change in gate voltage.

There are different tests to obtain required parameters.

**Parametric tests:**

The test environment can enable the user to monitor both actual change and percent change in their choices. ( $V_t$ ,  $I_{dlin}$ ,  $I_{dsat}$ ,  $I_{doff}$ ,  $I_{g(max)}$ ,  $g_m(I_d)$ ,  $V_g(I_d)$ ,  $I_{sub}$ )

**Parametric test description:**

(1).  $I_{dlin}$ : Drain current in liner region. (See figure 1)  
Setting drain voltage (in liner region) and gate voltage, measuring the drain current. Typically this  $I_{dlin}$  is measured with the gate voltage at operation voltage ( $V_{dd}$ ) for technology and drain voltage at 0.1V.  
*Input:*  $V_{ds}(0.1)$ ;  $V_{gs}(V_{dd})$

(2).  $I_{dsat}$ : Drain current in saturation region. (See Figure 1)  
Setting drain voltage (in saturation region) and gate voltage, measuring the drain current. Typically this  $I_{dsat}$  is measured with the gate and drain voltage equally at operation voltage ( $V_{dd}$ ) for technology.  
*Input:*  $V_{ds}(V_{dd})$ ;  $V_{gs}(V_{dd})$

*Extension:*  $I_{dsat\_rev}$ : Reverse drain current in saturation region.  
(P Type parameter)  
*Input:*  $V_{ds}(V_{dd})$ ;  $V_{gs}(V_{dd})$

(4).  $I_{sub}$  Substrate current at specified drain, gate voltage. (See Figure 2)  
*Input:*  $V_d$ ,  $V_g$

*Extension:*  $I_{sub\_max}$ : Maximum substrate current at  $V_d$   
*Input:*  $V_d$ ,  $V_{g\_start}$ ;  $V_{g\_stop}$ .

(5).  $I_d$ : Drain current at specified drain and gate voltage.  
*Input:*  $V_d$ ,  $V_g$

*Extension:*  $I_{doff}$ : Drain leakage current measurement. (P type device parameter)  
Setting the drain to the saturation voltage (typically is operation voltage ( $V_{dd}$ ) for the technology) and  $V_g$  and  $V_{sub}$  to zero.  
*Input:*  $V_d(V_{dd})$ ;  $V_g(0)$ ;  $V_{sub}(0)$ .



- (6).  $I_g$  Gate current at specified  $V_d$ ,  $V_g$ ,  $V_{sub}$ . (See Figure 2)  
Setting a user defined drain and gate voltage, measuring the gate current.  
*Input:*  $V_d$ ,  $V_g$ ;  $V_{sub}$ .
- Extensions*  $I_{g(max)}$ : Maximum gate current.  
Setting a user defined drain voltage and stepping the gate voltage, measuring the gate current.  
*Input:*  $V_d$ ,  $V_{g\_start}$ ;  $V_{g\_stop}$ .
- (8).  $g_{m(I_d)}$  Transconductance for a specified target drain current  $I_d$ , (See Figure 3)  
 $g_{m(I_d)}$  is determined by first obtaining gate voltage at user specified target current, then determined from a least squares fit of twenty (or  $N > 20$ ) drain current measurements in the vicinity of target current ( $\pm 0.05V$ )  
*Input:*  $V_d$ ,  $I_{d\_target}$ ,  $V_{g\_start}$ ;  $V_{g\_stop}$ .
- Extensions*  $g_{m(max)}$ : Maximum Transconductance.  
Setting the drain voltage to operate in liner or saturate region, stepping the gate voltage, measuring the drain current and gate voltage each step. Generating a characterization curve. Finding the maximum slop of the curve.  
*Input:*  $V_d$ ;  $V_{g\_start}$ ;  $V_{g\_stop}$ .
- $V_g(I_d)$  Gate voltage required to produce a specified target drain current. ( $I_d$ ). Use a binary search technique to determined the target  $I_d$ .  
*Input:*  $V_d$ ,  $I_{dtarget}$ ,  $V_{g\_start}$ ;  $V_{g\_stop}$ .
- (9).  $V_t$ : Threshold voltage measure.  
Holding the drain at a special voltage, stepping the gate voltage ( $V_g$ ), at each step the gate voltage and drain current are measured.  
There are several way to find  $V_t$ . (Definition. is “Gate voltage at **strong inversion**”)  
(a). Constant current threshold voltage.  
*Vtsweep:* Sweeping the gate, once the gate voltage producing a drain current greater than the target current, this gate voltage is seen as the threshold voltage.  
*Input:*  $V_d$ ,  $I_{dtarget}$ ,  $V_{g\_start}$ ;  $V_{g\_stop}$ .
- (b). Extrapolate threshold voltage.  
 $V_{th}$  Determined from extrapolate or intercept gate voltage  $V_{gi}$  at maximum slope of the  $I_d - V_g$  curve.
- $$V_{th} = V_{gi} - \frac{V_d}{2}$$
- where:



$$V_{gi} = V_{g \max} - \frac{I_{d \max}}{g_{m \max}}$$

$V_{g \max}$ ,  $I_{d \max}$  are the maximum gate voltage and drain current for maximum gm ( $g_{m \max}$ ).

$V_{th}$  can be divided as linear and saturate extrapolation threshold voltage when  $V_d$  is set to the linear (0.1V) and saturate operation ( $V_{dd}$ ) voltage respectively.

(c)  $V_t$  in the subthreshold method.

Subslp subthreshold slope is measured by the drain current measurement below threshold gate voltage, the slope is obtained from the plot as  $\log(I_d)$  vs.  $V_g$ . The subthreshold current depends linearly on  $V_g$  in such a semilog plot.

Normally finding a two  $V_g$  values corresponding to two target  $I_d$ . Then the  $V_g$  is stepping between two voltage limit, obtaining the slope from a least squares fit of  $\log(I_d)$ - $V_g$ .

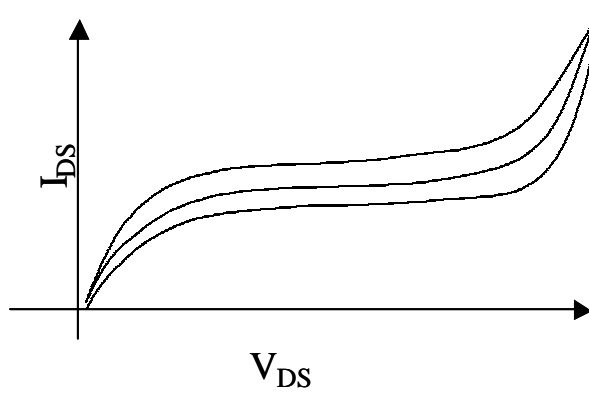
Some Definition:

$$g_m = dI_D / dV_{GS} | V_{GS} = V_{DS} = V_{dd}$$

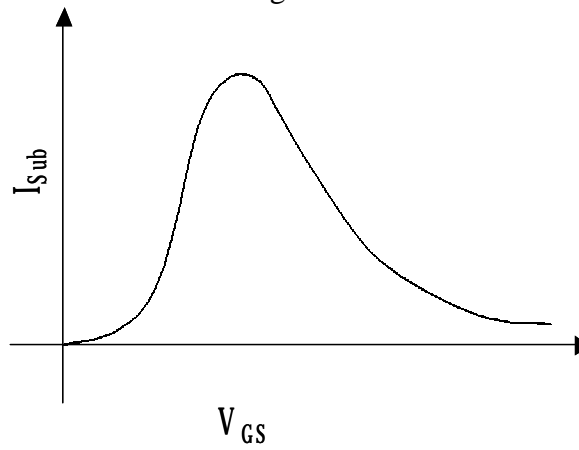
$$g_D = dI_D / dV_{DS} | V_{GS} = V_{DS} = V_{dd}$$

$$I_{off} = I_D | V_{GS} = 0, V_{DS} = V_{dd}$$

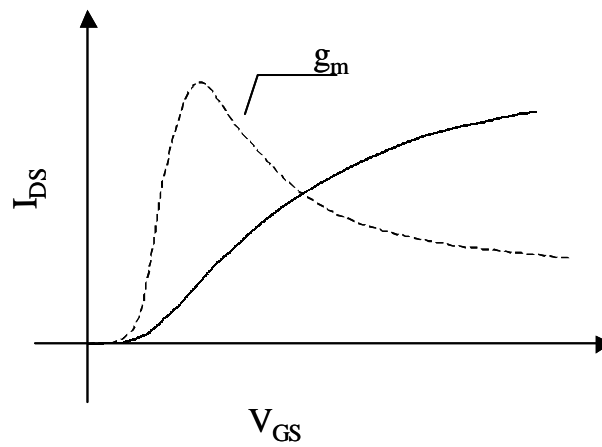
$$I_{sat} = I_{on} = I_D | V_{GS} = V_{DS} = V_{dd}$$



$V_{DS}$   
Figure 1



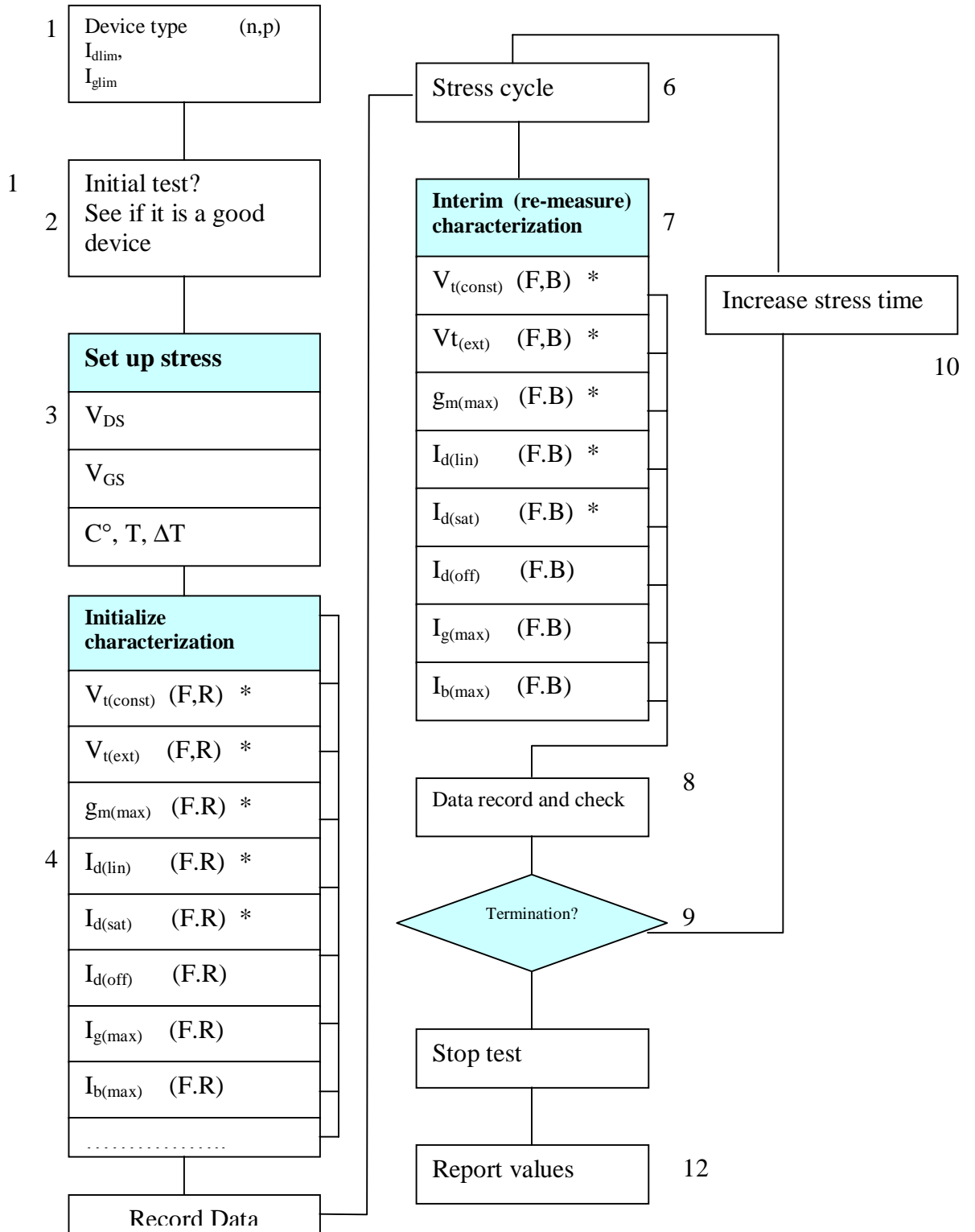
$V_{GS}$   
Figure 2



$V_{GS}$   
Figure 3



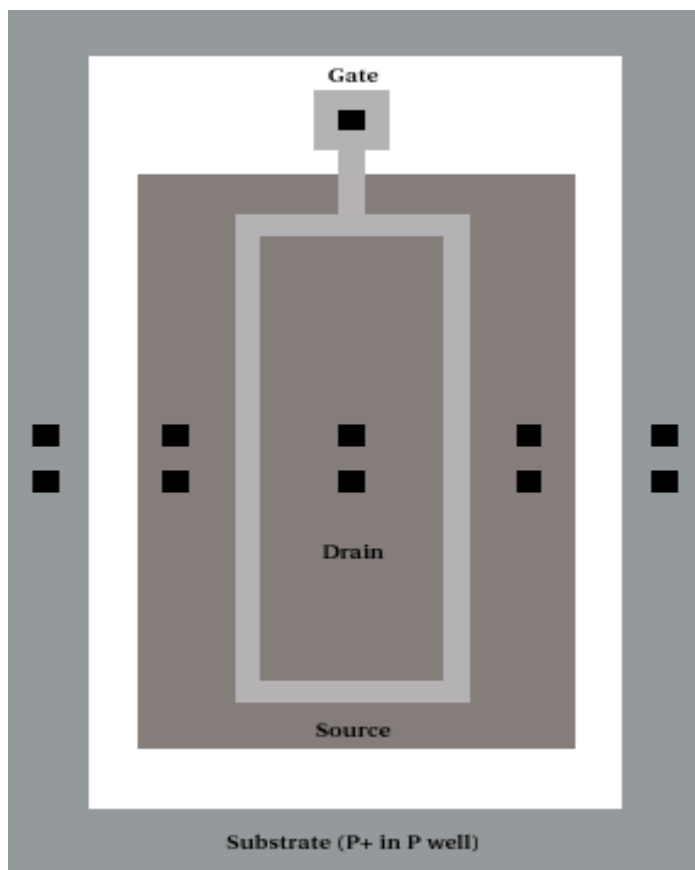
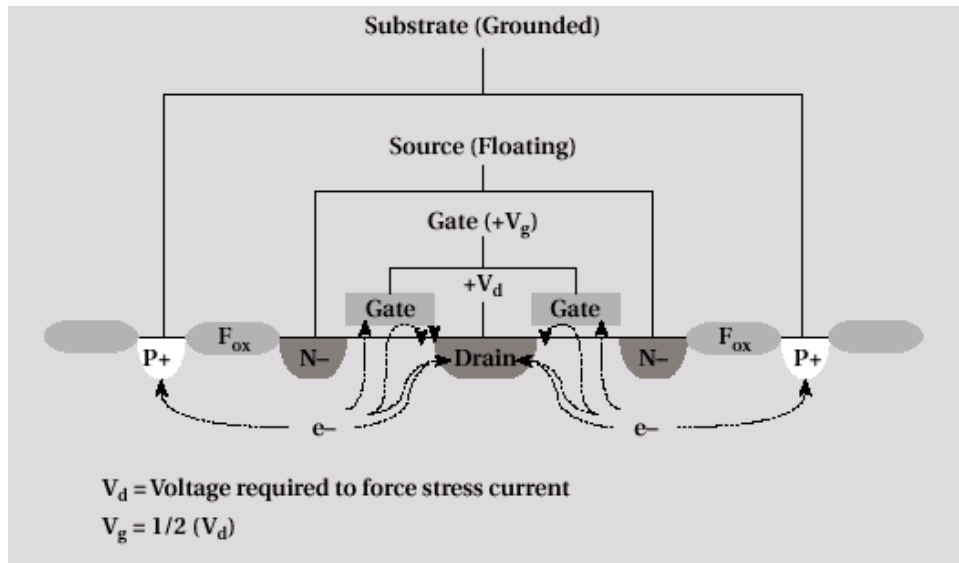
**Flow chart for HCI testing.**



\* The parametric tests required in JEDEC-28



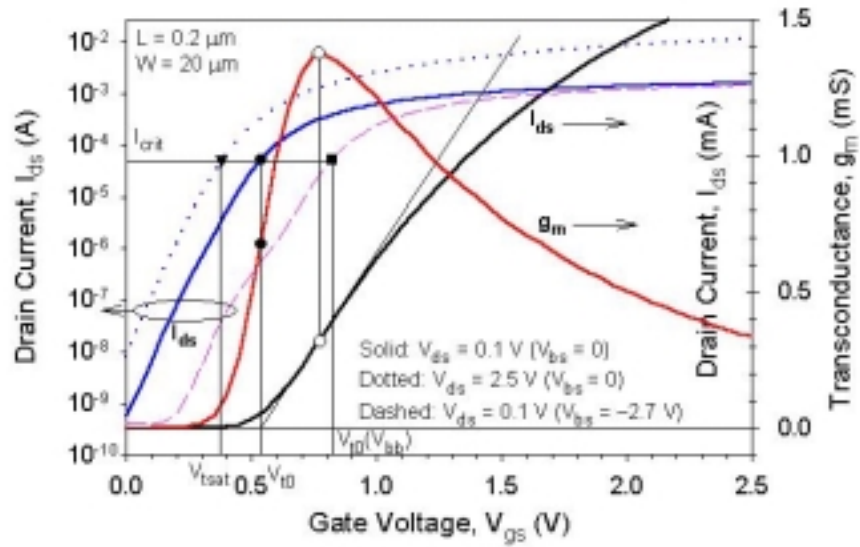
- 1 Device type: P or N type MOS device  
 $I_{dlim}$ : Drain Current Limit, the maximum drain current the user define for device, (mA)  
 $I_{glim}$  Gate Current Limit, the maximum gate current the user define (nA)
- 2
- 3  $V_{DS}$  Stress Drain voltage stress the user select (,90%  $V_{bd}$ )  
 $V_{GS}$  Stress Gate voltage stress (correspond to a maximum  $I_B$  for a  $V_{DS}$ )  
 $C^\circ, T$  Temperature stress and during time
- 4
- 6 Stress cycle: The device running under the stresses that are determined above. The stress voltage order is  $V_{BS} \rightarrow V_{GS} \rightarrow V_{DS}$ . Turn off device should be done in the revise order  $V_{DS} \rightarrow V_{GS} \rightarrow V_{BS}$ . The stress continues until a stress interval time has been reached.
- 7 The selected characterization (parameters) should be measured and recorded
- 8 The device should be stressed until at least one parameter reaches or exceed the target value, or two time decades of valid data has been taken.
- 12 N type:  $V_{DD}, V_{BB},$   
 $V_{DS} V_{GS}, V_{BS},$   
Initial  $I_B$  at stress current  
Initial  $I_{d(liner)} I_{d(sat)} g_{m(max)} V_t$   
Stress time  
 $V_D$



Test structure.



**Threshold Voltage Definition ( $I_{crit}@V_{t0}$ )**



Definition of threshold voltage: (maximum gm method)

- 1 from  $g_{m(max)}$  in linear range, ( $V_{ds}=0.1V$ )  $\rightarrow$  maximum slop  $\rightarrow$  slop line  $\rightarrow V_{t0}$ :
- 2 Got three lines,  $\log I_{ds}-V_{gs}$ , ( $V_{bs}=0, V_{ds}=0.1$ ); ( $V_{bs}=0, V_{ds}=V_{DD}$ ); ( $V_{bs}=V_{DD}, V_{ds}=0.1$ ),
- 3 From  $V_{t0} \rightarrow I_{crit}$  @ ( $V_{bs}=0, V_{ds}=0.1$ )  $\rightarrow V_{tstart}$  @ ( $V_{bs}=0, V_{ds}=V_{DD}$ )  $\rightarrow V_{t0}(V_{DD})$  @ ( $V_{bs}=V_{DD}, V_{ds}=0.1$ )



**What is not HOC effect?**

When a MOSFET acts as a good switch, the drain-source current is as large as possible in the on state and very low in the off state. The typical effect of hot- carrier, or commonly hot- electron, degradation is to reduce the on- state current in an n- MOSFET and increase the off- state current in a p- MOSFET.

For semiconductors in thermal equilibrium, electrons and holes continually absorb and emit acoustical phonons (low- frequency lattice vibrations), resulting in an average energy gain of zero. Such electrons have kinetic energies that are normally slightly higher than that of the conduction band edge by an amount  $-kT_r$ . Similarly, for holes,  $E$  is slightly less than the valence band edge again by  $-kT_r$ .

At room temperature ( $T_r$ ),  $kT_r$  is only 0.025 eV, which is small compared to the carrier kinetic energy corresponding to  $E_c$  and  $E_v$ . This is the case in low electric fields, where the carrier velocity is field- independent (Ohm's law).