



Modified VRAMP Test (with SILC)

Modified VRAMP testing is a method to evaluate Stress Induced Leakage Current (SILC) of thin oxides. It is a modified module of VRAMP. The testing procedure is similar to the voltage ramp testing, additional with the low voltage measurements during the voltage ramp. The testing provide charge-to-breakdown (Q_{bd}) and the SILC information after stress.

Stress Induced Leakage Current

Stress Induced Leakage Current (SILC) is leakage through a thin gate oxide due to tunneling into and out of traps in the oxide. This leakage is measured using capacitor test structures. The leakage is induced by tunneling current stress in the thin dielectric and, therefore, is called Stress Induced Leakage Current. Figure 1 shows the leakage through a thin dielectric before and after a short tunneling current stress.

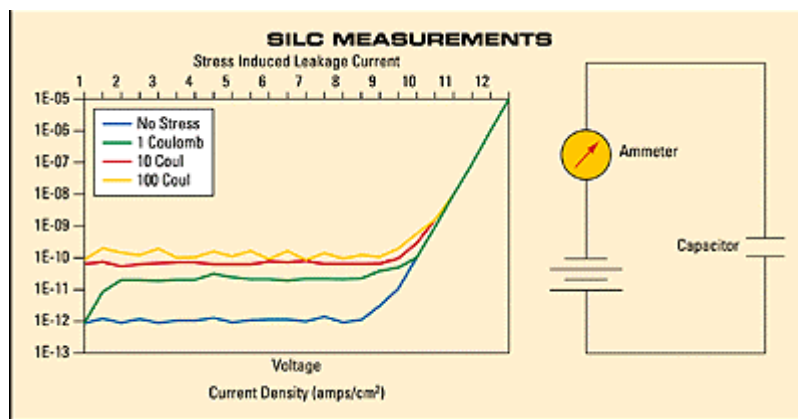


Figure1. The leakage through a thin dielectric prior to and following a short tunneling current stress is shown. When additional stress is applied, the leakage value quickly saturates. The figure shows current density (A/cm^2), not actual current.

The modified voltage ramp test is based on the voltage ramp test. It starts at usage voltage V_{start} and ramps voltage linearly until the breakdown occurs. During the ramping, the voltage periodically returns to a low level and measure the leakage current correspondingly. Figure 1 shows the voltage ramping in the test.

Test Descriptions:

- Pre-Ramp oxide current test
This is to determine initial oxide integrity.
This test applies a bias V_{use} and measure the leakage oxide current, if the current $I_{use-pre}$ exceeds the fail current I_{init} , then the test termination.
- Ramp voltage stress and return back to low voltage.
A linear or stepped voltage ramp is applied in this test. The voltage starts as V_{start} and ramps at a predefined ramp rate. At each voltage step the measured current should be compared to the oxide breakdown criterion. If breakdown has not occurred, the Q_{bd} (accumulated oxide charge) should be recalculated. The SLIC information obtained is



accomplished by low voltage measurements during ramping. The SMU force a low voltage and measure the current. After breakdown occur, the leakage current is checked again.

- **Post-ramp oxide current test.**
Once the voltage ramp is completed, the test then forces the use_voltage again and measures the leakage current. This test is performed to determine the final state of the test device. Based on these test results, the oxide failure category is then determined.

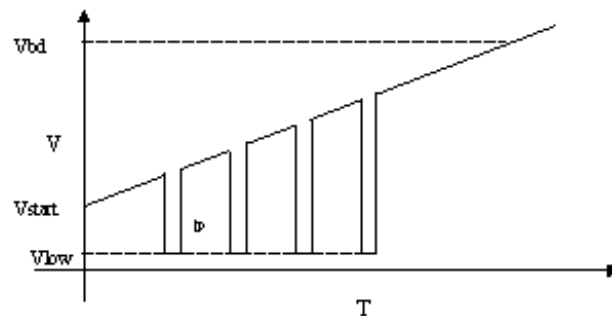


Figure 1. Voltage ramp at modified VRAMP testing

Input variables:

<i>Parameters</i>	<i>Default value</i>
use_voltage - pre and post-stress applied test voltage (V)	
check_current - pre and post-stress check current (A)	
use_voltage_delay - pre and post-stress measurement and first voltage step delay (ms)	
start_voltage - starting ramp voltage (V)	
final_voltage - maximum ramp voltage (V)	
step_voltage - voltage ramp step size (V)	
step_delay - duration of each step in the voltage ramp (typ. value: 40-100)(ms)	100ms
sample_rate - measurement sampling rate (< step delay) (ms)	10ms
fail_current - fail Current (mA)	100mA
exit_curr_mult - exit current multiplier. See Note2. (typ. value: 10-100)	10
max_time - time limit on ramp (s)	20s
charge_limit - charge limit (C/cm ²)	
area - area of oxide structure (cm ²)	
leakage_voltage - force low voltage to check SLIC (V)	0.5
check_rate - checking rate of low voltage forcing. (S)	1

Output variables:

Qbd	Charge breakdown, Vbd	voltage breakdown, Ibd	current	breakdown,	TTF
	time to breakdown. SLIC at different ramping stage.				