Centaur

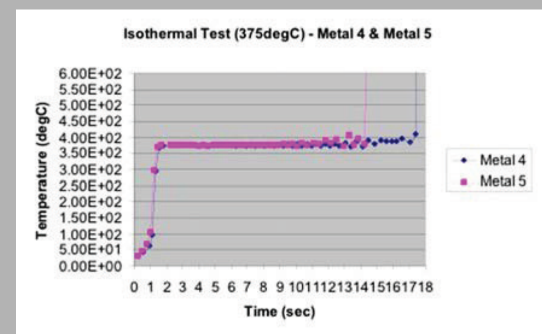
Wafer Level Reliability Test System

Fully Automated Deep Submicron Wafer Level Reliability Evaluation System

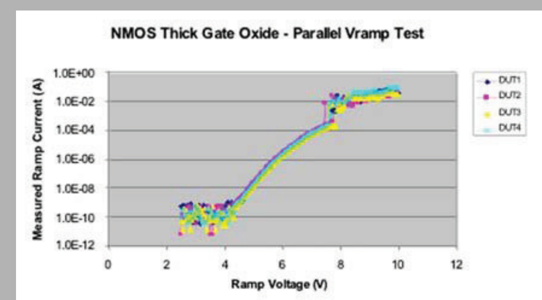
Key Features

- *true-parallel* test architecture, up to 8 SMUs or Voltage Sources supported over one system, enabling parallel testing for up to 8 DUTs or more at the same time
- Integrated turnkey parallel test solution with proprietary design low leakage (<10fA) and high temperature (400°C) multiple sites probe card assembly
- Utilised proprietary design low leakage Switch Matrix Cards (<10fA) to achieve fully Kelvin SMUs switching for increased parallel capability
- Fully guarded for high speed and low current
- High speed parallel switching
- Full integration with industry's latest model semi-auto and automatic probe stations
- Allows separate test program definition per site, sub-site and wafer
- Window XP based, dynamic and user friendly software for test, data analysis and report generation
- Support SQL commands for test descriptions to allow automatic test program generation and minimum engineering time
- Supports the following reliability evaluation per various Industry Standards;
  - Voltage-ramp Method per JESD No. 35, "Procedure for the Wafer Level Testing of Thin Dielectrics"
  - Current-ramp Method per JESD No. 35, "Procedure for the Wafer Level Testing of Thin Dielectrics"
  - "Traditional Voltage-ramp and Modified Voltage-ramp Method (pulsed staircase sweep)", test up to 6 test structures in parallel
  - Isothermal Electromigration Testing (JEDEC Compliant) test up to 6 test structures in parallel
  - Poly Heated Via and Contact Electromigration Testing
  - Time Dependent Dielectric Breakdown (Constant Voltage), test up to 40 test structures in parallel
  - High Voltage Time Dependent Dielectric Breakdown for ILD
  - Mechanical Fracture of Interlevel Dielectric (ILD)
  - Junction Leakage
  - Hot Carrier Degradation (HCI) and Negative Bias Temperature Instability (NBTI), test up to 6 test structures in parallel
  - Charge to Breakdown (Q_{bd})
  - Mobile Ion measurements using Triangular Voltage Sweep (TVS)

Centaur integrates with both TSK UF3000 12"inch Auto prober and Cascade S300 12"inch Semi Auto Prober



Parallel ISOEM test (Constant Power Mode). Two metal lines tested with the JEDEC Standard using TCR to compute structure target temperature



Parallel VRAMP test (four NMOS thick gate oxides tested in parallel)

- Stress Induced Leakage Current (SILC)
- Process Plasma Induced Damage (PPID)
- Stress Migration for Lines and Vias
- Tin Whisker Growth
- Ball Bond Integrity
- Solder Bump Electromigration

- Ability to perform parametric measurements
- Extraction of measurement data into common spreadsheet and data analysis programs such as Microsoft Office Excel
- Ability to enter variable names from a “technology” file of variable names and equations in place of numbers as part of the test description

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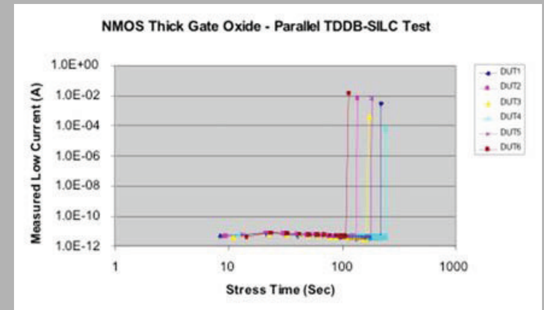
In today’s highly competitive business environment, semiconductor manufacturers have to significantly reduce their product time to market and develop their technology at a fraction of cost, while meeting or exceeding the ever demanding quality and reliability expectations of their customers. The situation is even more acute when it comes to deep submicron technology, where new materials like, Ultra Thin Gate Oxide, Copper (Cu) metallization and low-K dielectrics are used. The chances for a first time success are highly dependent on how quickly the performance of these new materials and process options are understood, especially how their reliability are characterized. Chiron offers the Centaur which is fully automated. This Parallel Deep Submicron Reliability Evaluation System fills the gap by offering the industry first *true-parallel* wafer level reliability test system. It supports various industry standard methods for thin & thick dielectric reliability tests, including the JEDEC Standards.

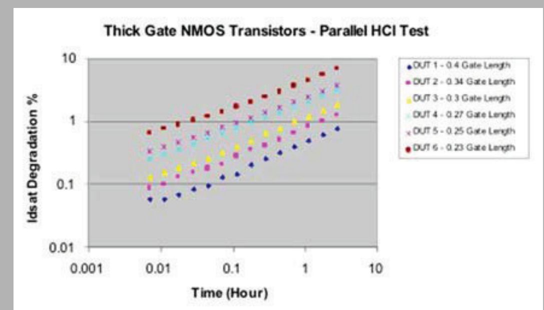
true-parallel

Chiron’s Centaur flexible architecture allow configurations that start at one single Source Measurement Unit (SMU) and range up to 8 SMUs in one system. This *true-parallel* architecture allows tests to be carried out simultaneously on all DUTs connected via the probe card. Besides a significant improvement in the test throughput, this architecture eliminates the need for a switch matrix, hence improving tremendously on the low level current measurements. Flexibility can also be achieved with lower number of SMUs or sources, when integrated with both Chiron’s proprietary low leakage switch matrix and high temperature multiple-site probe card.

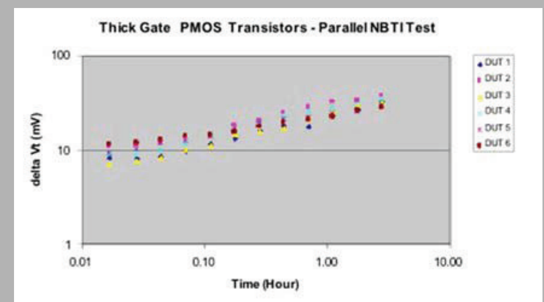
The unique Centaur solutions, besides tapping from the industry leaders in their hardware precision, providing flexibility and user-friendliness software environment. Most of the work that a Reliability or Device Engineer could ever dream of doing is provided in an intuitive and user-friendly manner. For example, a typical JESD No. 35 test, along with data analysis and results presentation preference can be fully set-up and run in a mere 10 minutes. All test set-up and data can be saved and managed by powerful database management software onboard the system. With such solution, the engineers can spend more time on solving engineering problems, improving product and process yield, quality and reliability rather than on developing test programs and test hardware.



Parallel TDDB SILC test (six NMOS thick gate oxides tested in parallel)



Parallel HCI test (six NMOS thick gate transistors with 6 different gate lengths tested in parallel)



Parallel HCI test (six PMOS thick gate transistors with 6 same gate lengths tested in parallel)

CHIRON Technology Pte Ltd
23 Woodlands Terrace #03-00, Singapore 738472
Tel: (65) 6555 5260 Fax: (65) 6555 5265
Svc Hotline: (65) 6555 5238
E-mail: sales@chironholdings.com Website: www.chironholdings.com